The Abdus Salam International Centre for Theoretical Physics

IAEA International Atomic Energy Agency

unesco United Nations Educational, Scientific and Cultural Organization

STINT 2026

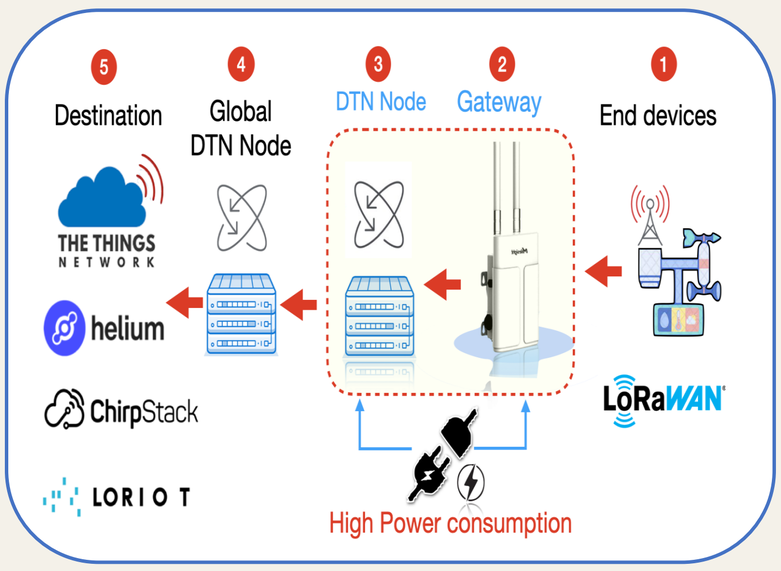
Ultra Low-Power DTN Framework for LoRaWAN®

Moez Altayeb

PhD, Postdoc @ ICTP (03-2026) Trieste, Italy

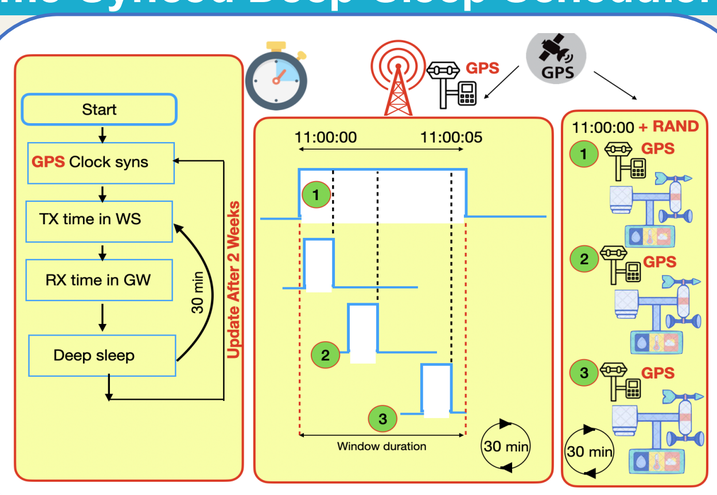
Main issue and proposed solution

Integrated DTN Node within LoRaWAN Gateway Chain and highlights the power-hungry stages.



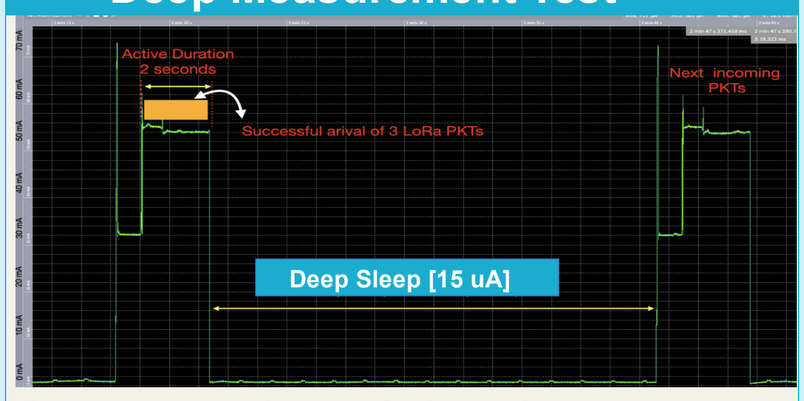
- Ultra-Low-Power Framework:
- Custom DTN Bundle Architecture
- Novel Power Reduction Algorithms
- Low-Power LoRaWAN Architecture
- Machine Learning-Driven Power Optimization.

Time-Synced Deep-Sleep Scheduler



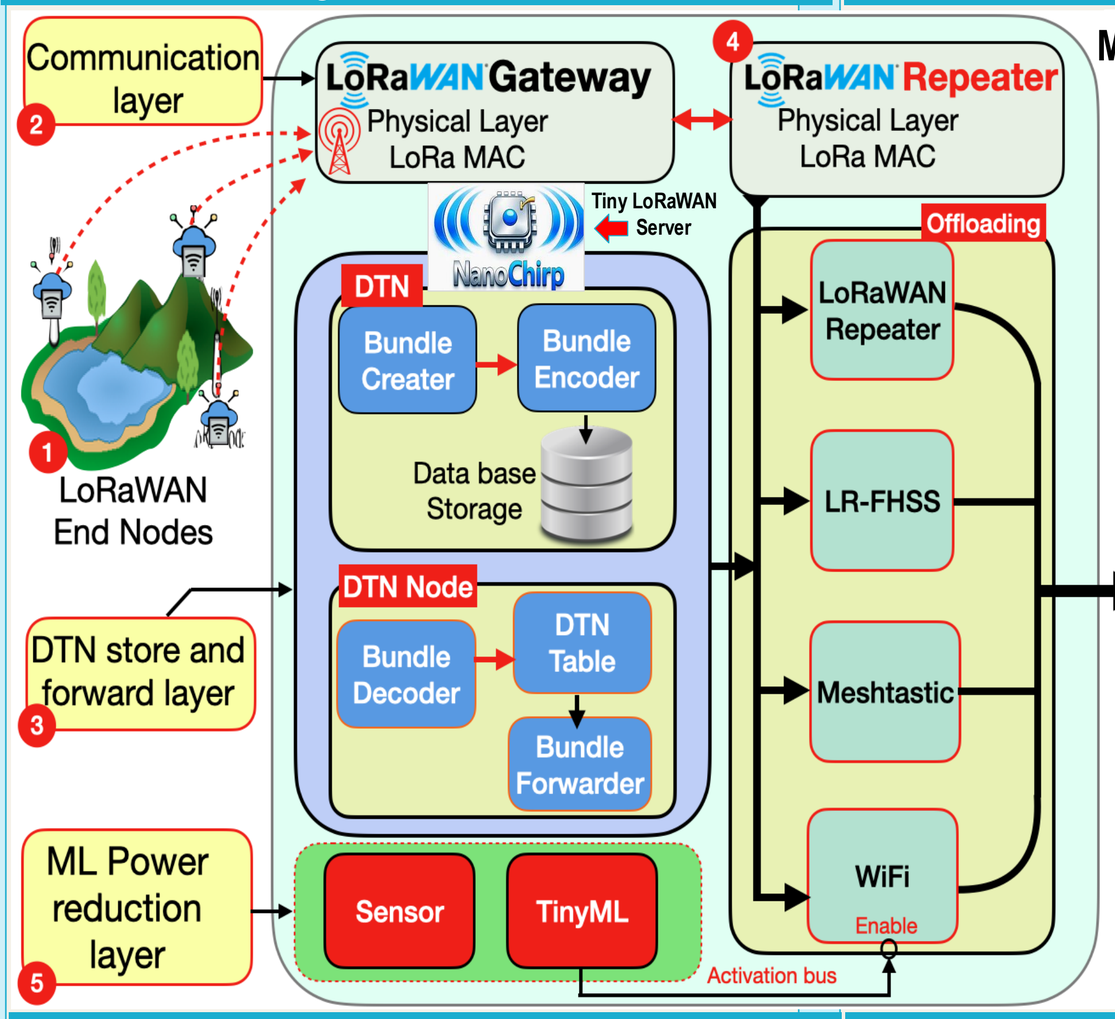
- Gateway and end-nodes share the same global clock and
- time-table for sleep and wake up
- Gateway opens the communication window at the exact
- scheduled time.
- End-nodes wake at the same window and send their pkts
- Both of gateway and end nods goes to deep sleep and so on,

Deep Measurement Test



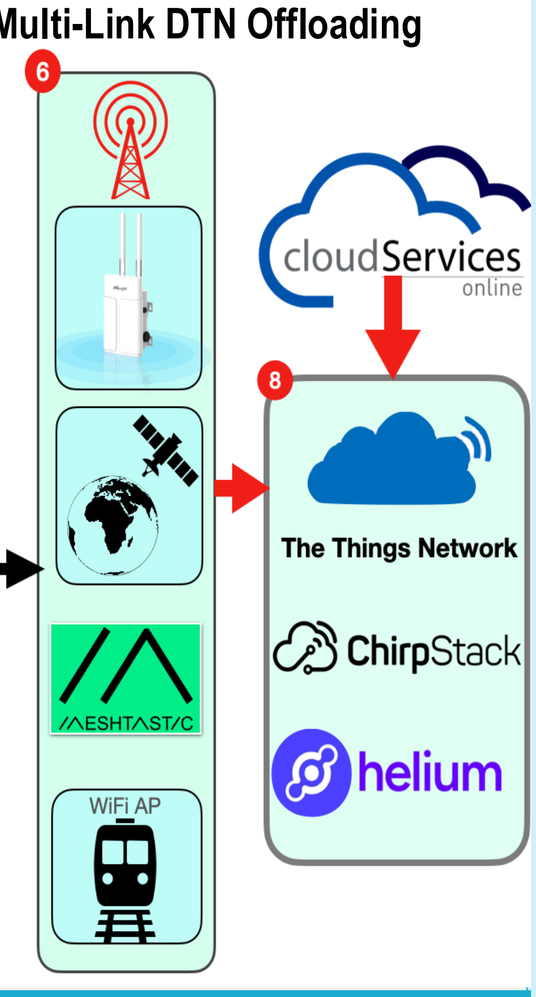
Power consumption result shows the system can woks for ~ 5 years with tiny 3.6v, 19 Ah battery

System Architecture

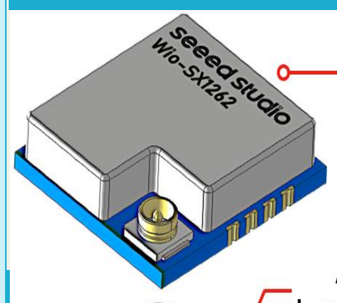


Destination

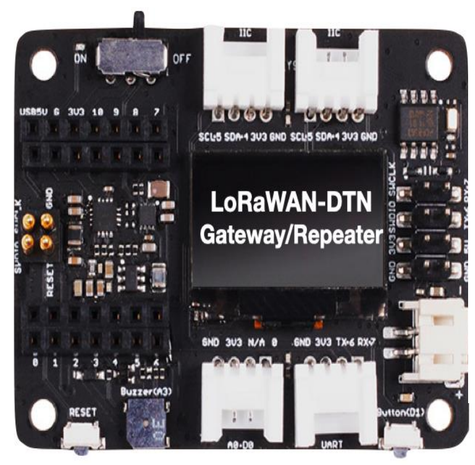
Multi-Link DTN Offloading



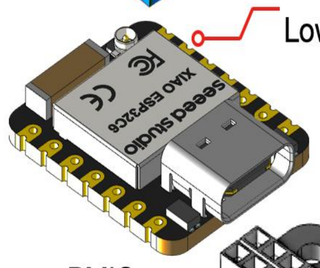
Prototype System



LR1121/SX1262 Super low-power LoRa LR-FHSS modem

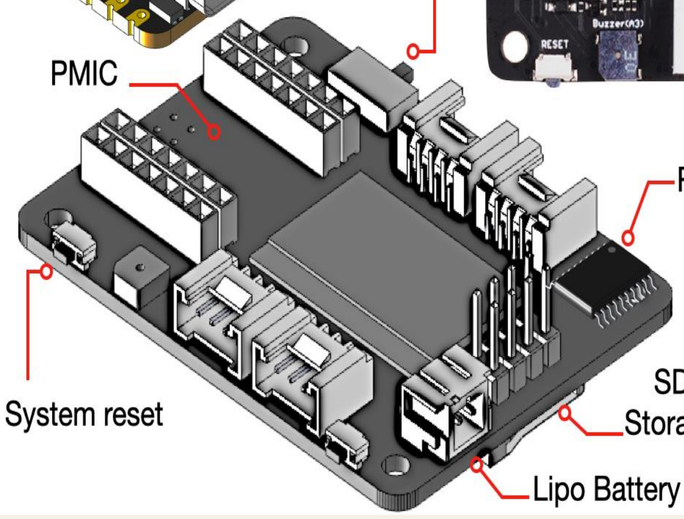


Advanced Low-power CPU



Battery SW

PMIC



RTC Unit/ Battery



System reset

SD Storage

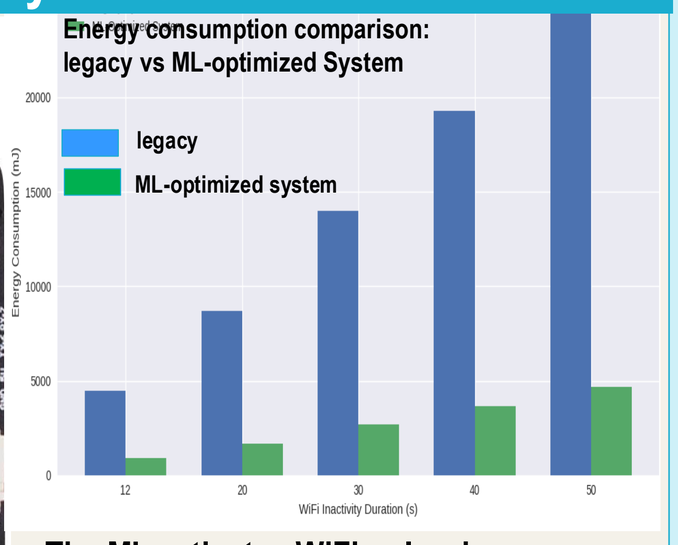


Lipo Battery input

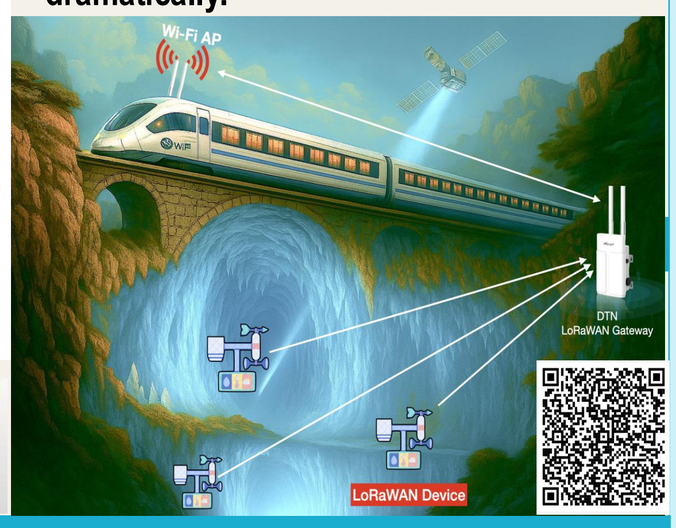
Ultra-low power hardware CPU and Modem operates on tiny battery.

Final HW will be in FPGA

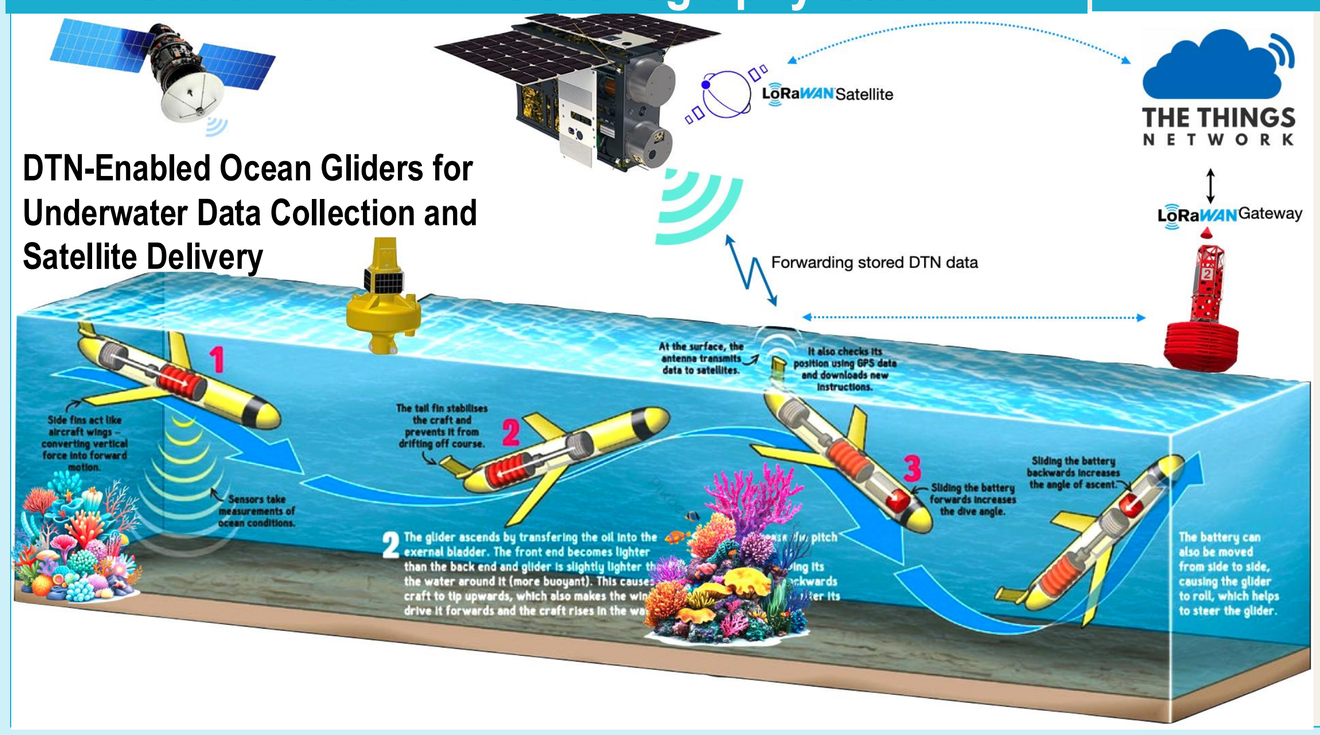
TinyML for Power Reduction



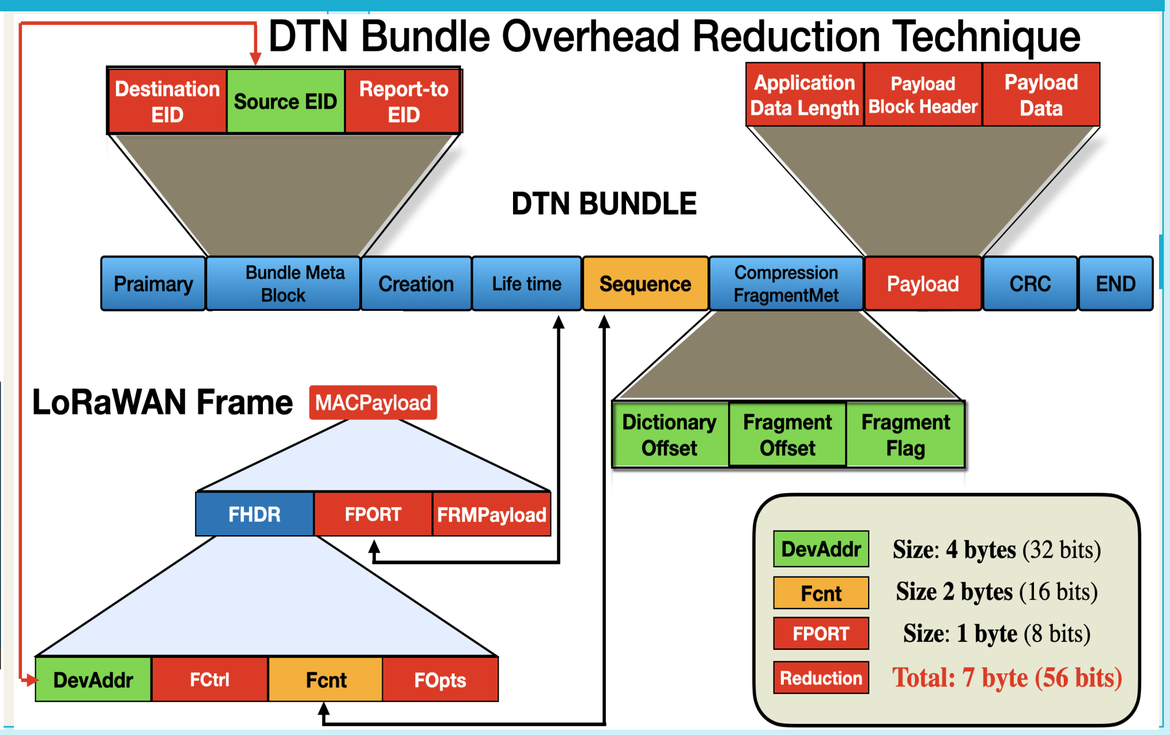
TinyML activates WiFi only when needed, reducing power consumption dramatically.



Underwater DTN Oceanography Glider



LoRaWAN-Aware DTN Bundle Architecture



Poster template by ResearchPosters.co.za